FAIRCHILD SEMICONDUCTOR®

FSDM311

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Precision Fixed Operating Frequency (67kHz)
- Advanced Burst-Mode operation Consumes under 0.2W at 265Vac and no load
- Internal Start-up Switch and Soft Start
- Under Voltage Lock Out (UVLO) with Hysteresis
- Pulse by Pulse Current Limit
- Over Load Protection (OLP)
- Over Voltage Protection (OVP)
- Internal Thermal Shutdown Function (TSD)
- Secondary Side Regulation
- Auto-Restart Mode

Applications

- Charger & Adaptor for Mobile Phone, PDA & MP3
- Auxiliary Power for White Goods, PC, C-TV & Monitor

Description

The FSDM311 is an integrated Pulse Width Modulator (PWM) and Sense FET specially designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. This device is a monolithic high voltage power switching regulator which combines an VDMOS Sense FET with a voltage mode PWM control block. The integrated PWM controller features include: a fixed oscillator, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), optimized gate turn-on/ turn-off driver, thermal shut down protection (TSD), temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDM311 reduces total component count, design size, weight and at the same time increases efficiency, productivity, and system reliability. This device is a basic platform well suited for cost effective designs of flyback converters.

TYPICAL POWER CAPABILITY		
PRODUCT	Open Frame	
	230VAC ±15%(1)	85-265VAC
FSDM311	20W	12W
FSDM311L	20W	12W

Table 1. Notes: 1. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

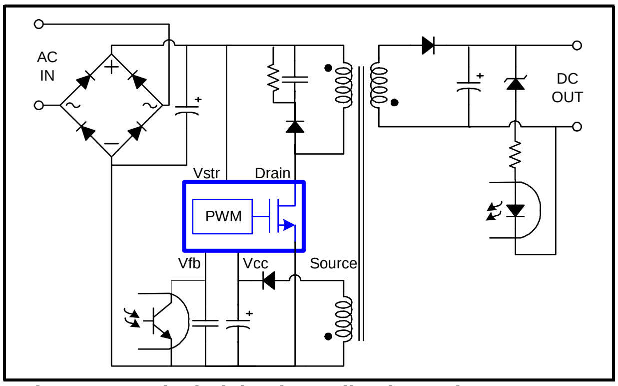


Figure 1. Typical Flyback Application using FSDM311

Rev.1.0.4

Internal Block Diagram

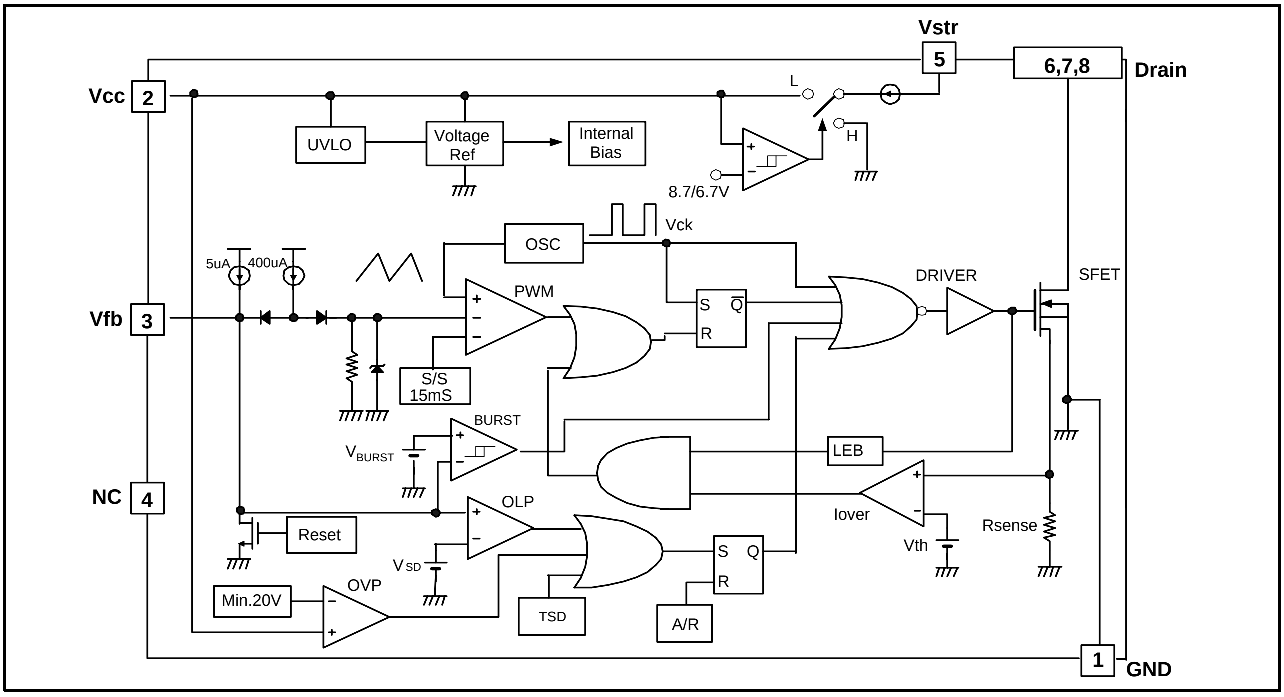


Figure 2. Functional Block Diagram of FSDM311

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 8 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (8.7V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the inverting input to the PWM comparator with nominal input levels between 0.5Vand 2.5V. It has a 0.40mA current source connected internally while a capacitor and opto coupler are typically connected externally. A feedback voltage of 4.5Vtriggers overload protection (OLP). There is a time delay while charging between 3V and 4.5V using an internal 5uA current source, which prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
5	Vstr	The startup pin connects directly to the rectified AC line voltage source for FSDM311. For the FSDM311, at start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once this reaches 9V, the internal current source is disabled.
6, 7, 8	Drain	The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V. Minimizing the length of the trace connecting this pin to the transformer will decrease leakage inductance.

Pin Configuration

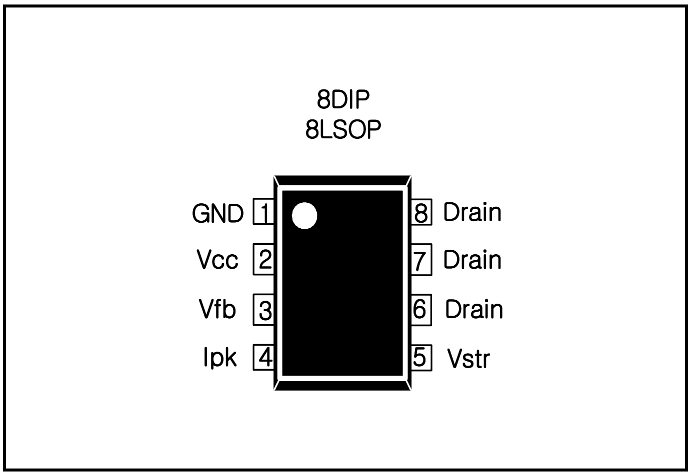


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Maximum Vstr Pin Voltage	$V_{STR,MAX}$	650	V
Maximum Drain Pin Voltage	$V_{DRAIN,MAX}$	650	V
Drain-Gate Voltage (R_{GS}=1MΩ)	V_{DGR}	650	V
Gate-Source (GND) Voltage	V_{GS}	±20	V
Drain Current Pulsed (1)	I_{DM}	1.5	A_{DC}
Continuous Drain Current (Tc=25°C)	I_D	0.5	A_{DC}
Continuous Drain Current (Tc=100°C)	I_D	0.32	A_{DC}
Single Pulsed Avalanche Energy (2)	E_{AS}	10	mJ
Maximum Supply Voltage	$V_{CC,MAX}$	20	V
Input Voltage Range	V_{FB}	–0.3 to Vstop	V
Total Power Dissipation	P_D	1.25	W
Operating Junction Temperature.	T_J	+150	°C
Operating Ambient Temperature.	T_A	-25 to +85	°C
Storage Temperature Range.	T_{STG}	-55 to +150	°C

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L=24mH, starting Tj=25°C

Thermal Impedance

Parameter	Symbol	Value	Unit
8DIP			
Junction-to-Ambient Thermal	θ_{JA}(1)	?(3)	°C/W
	θ_{JA}(1)	?(4)	°C/W
Junction-to-Case Thermal	θ_{JC}(2)		°C/W

Note:
1. Free standing without heatsink.
2. Measured on the GND pin close to plastic interface.
3. Soldered to 100mm^2 copper clad.
4. Soldered to 300mm^2 copper clad.

Electrical Characteristics (Sense FET Part)

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=50μA	650	720	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=Max. Rating, V_{GS}=0V	-	-	25	μA
		V_{DS}=0.8Max. Rating, V_{GS}=0V, T_C=125°C	-	-	200	μA
Static Drain-Source on Resistance (Note)	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.5A	-	14	19	Ω
Forward Trans conductance (Note)	gfs	V_{DS}=50V, I_D=0.5A	1.0	1.3	-	S
Input Capacitance	C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	162	-	pF
Output Capacitance	C_{OSS}		-	18	-	
Reverse Transfer Capacitance	C_{RSS}		-	3.8	-	
Turn on Delay Time	td(on)	V_{DD}=0.5B V_{DSS}, I_D=1.0A (MOSFET switching time is essentially independent of operating temperature)	-	9.5	-	ns
Rise Time	tr		-	19	-	
Turn Off Delay Time	td(off)		-	33	-	
Fall Time	tf		-	42	-	
Total Gate Charge (Gate-Source + Gate-Drain)	Qg	V_{GS}=10V, I_D=1.0A, V_{DS}=0.5B V_{DSS} (MOSFET switching time is essentially independent of operating temperature)	-	7.0	-	nC
Gate-Source Charge	Qgs		-	3.1	-	
Gate-Drain (Miller) Charge	Qgd		-	0.4	-	

Note:

1. Pulse test: Pulse width ≤ 300μS, duty ≤ 2%
2. $S = \frac{1}{R}$

Electrical Characteristics (Control Part) (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
UVLO SECTION						
Start Threshold Voltage	V_{START}	V_{FB}=GND	8	9	10	V
Stop Threshold Voltage	V_{STOP}	V_{FB}=GND	6	7	8	V
OSCILLATOR SECTION						
Initial Accuracy	F_{OSC}		61	67	73	kHz
Frequency Change With Temperature (2)	ΔF/ΔT	-25°C ≤ Ta ≤ +85°C	-	±5	±10	%
Maximum Duty Cycle	Dmax		60	67	74	%
FEEDBACK SECTION						
Feedback Source Current	I_{FB}	Ta=25°C, 0V ≤ Vfb ≤ 3V	0.35	0.40	0.45	mA
Shutdown Feedback Voltage	V_{SD}		4.0	4.5	5.0	V
Shutdown Delay Current	I_{DELAY}	Ta=25°C, 3V ≤ Vfb ≤ V_{SD}	4	5	6	µA
BURST MODE SECTION						
Burst Mode Voltage	V_{BURH}	Tj = 25°C	0.6	0.70	0.8	V
	V_{BURL}		0.45	0.55	0.65	V
	Hysteresis		-	150	-	mV
REFERENCE SECTION						
Output Voltage (1)	Vref	Ta=25°C	4.20	4.50	4.80	V
Temperature Stability (1)(2)	Vref/ΔT	-25°C ≤ Ta ≤ +85°C	-	0.3	0.6	mV/°C
CURRENT LIMIT(SELF-PROTECTION)SECTION						
Peak Current Limit	I_{OVER}		0.475	0.55	0.625	A
SOFT START SECTION						
Soft Start Time	T_{SOFT}		10	15	20	ms
PROTECTION SECTION						
Thermal Shutdown Temperature (1)	T_{SD}	-	125	145	-	°C
Over Voltage Protection	V_{OVP}		20	-	-	V
TOTAL STANDBY CURRENT SECTION						
Start-up Current	I_{STR}	V_{CC}=0V, V_{STR}=50V	450	550	650	µA
Operating Supply Current (Control Part Only)	I_{OP}	V_{CC} ≤ 16	-	1.5	3.0	mA

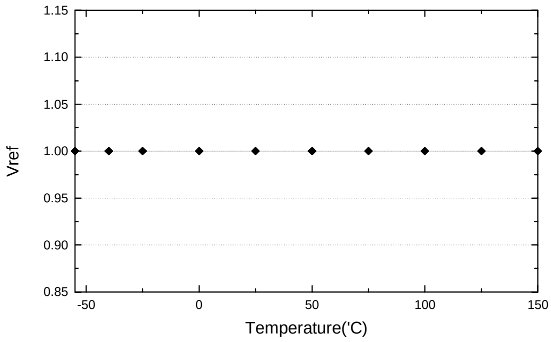
Note:
1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process

Comparison Between FSDH0165 and FSDM311

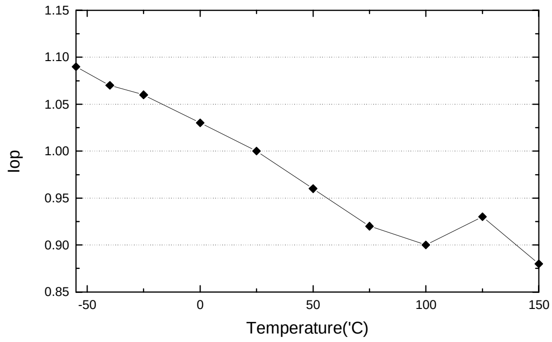
Function	FSDH0165	FSDM311	FSDM311 Advantages
Soft-Start	not applicable	15mS	• Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
Burst Mode Operation	not applicable	Yes-built into controller	• Improve light load efficiency • Reduces no-load consumption • Transformer audible noise reduction
Drain Creepage at Package	1.02mm	3.56mm DIP 3.56mm LSOP	• Greater immunity to arcing as a result of build-up of dust, debris and other contaminants

Typical Performance Characteristics

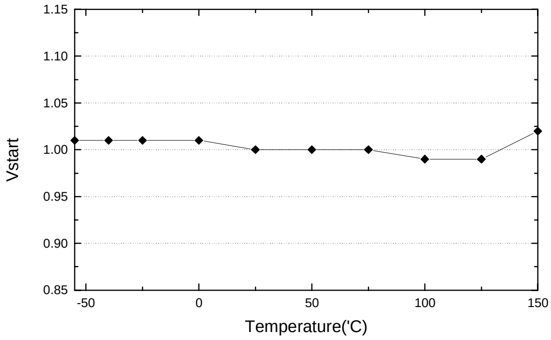
(These characteristic graphs are normalized at Ta=25°C)



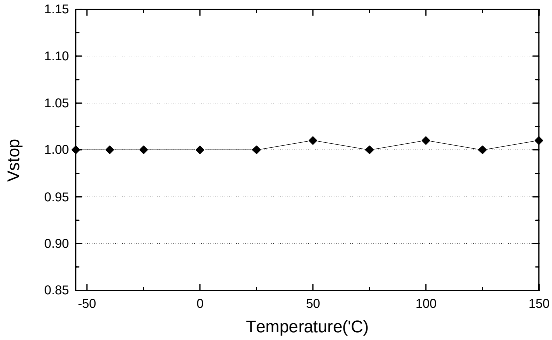
Reference Voltage vs. Temp



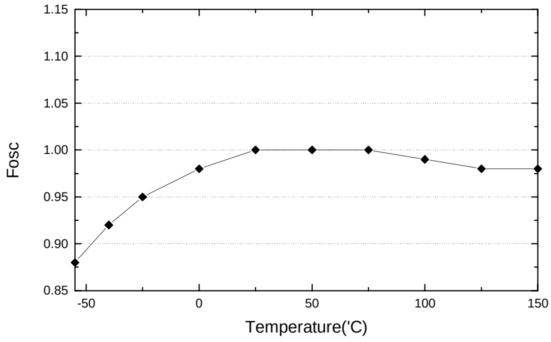
Operating Current vs. Temp



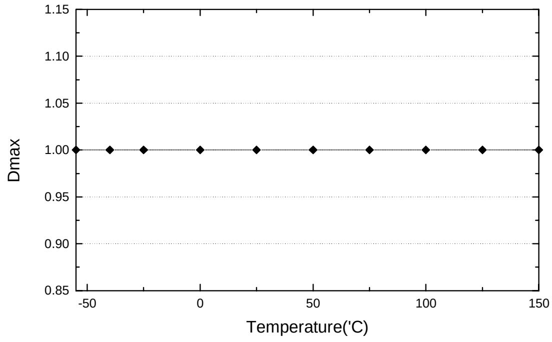
Start Threshold Voltage vs. Temp



Stop Threshold Voltage vs. Temp



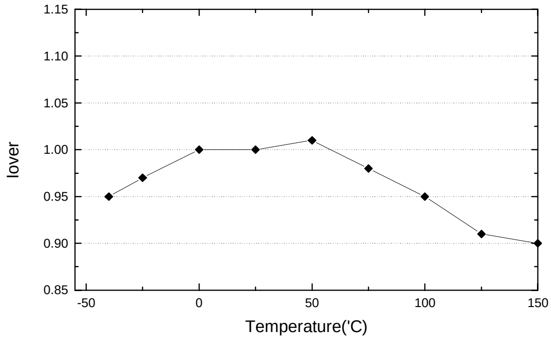
Frequency vs. Temp



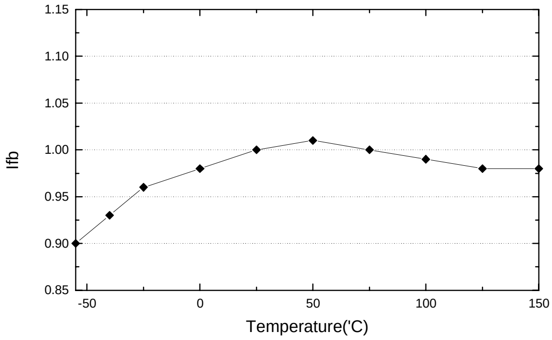
Maximum Duty vs. Temp

Typical Performance Characteristics (Continued)

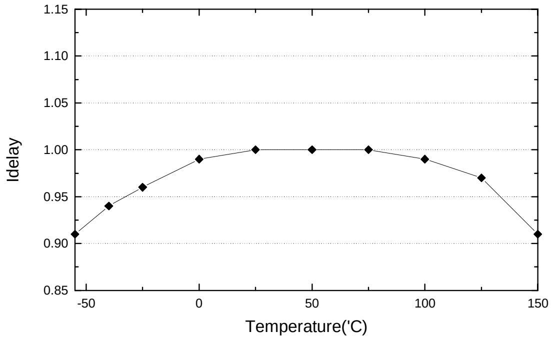
(These characteristic graphs are normalized at Ta=25°C)



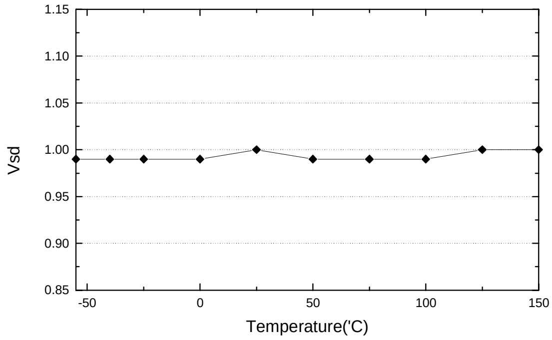
Peak Current Limit vs. Temp



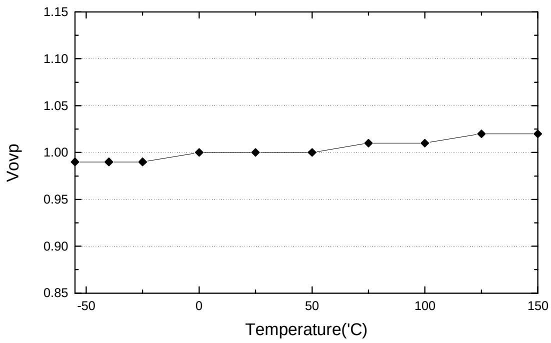
Feedback Source Current vs. Temp



ShutDown Delay Current vs. Temp



ShutDown Feedback Voltage vs. Temp



Over Voltage Protection vs. Temp

Functional Description

1. Startup : At startup, the internal high voltage current source supplies the internal bias and charges the external Vcc capacitor as shown in Figure 4. In the case of the FSDM311, when Vcc reaches 9V the device starts switching and the internal high voltage current source is disabled. The device continues to switch provided that Vcc does not drop below 7V. After startup the bias is supplied from the auxiliary transformer winding.

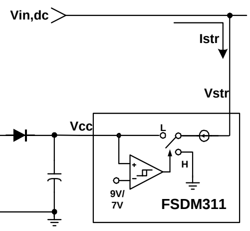


Figure 4. Internal startup circuit

Calculating the Vcc capacitor is an important step to designing in the FSDM311. At initial start-up in the FSDM311, the stand-by maximum current is 100uA, supplying current to UVLO and Vref Block. The charging current (i) of the Vcc capacitor is equal to Istr - 100uA. After Vcc reaches the UVLO start voltage only the bias winding supplies Vcc current to device. When the bias winding voltage is not sufficient, the Vcc level decreases to the UVLO stop voltage. At this time Vcc oscillates. In order to prevent this ripple it is recommended that the Vcc capacitor be sized between 10uF and 47uF.

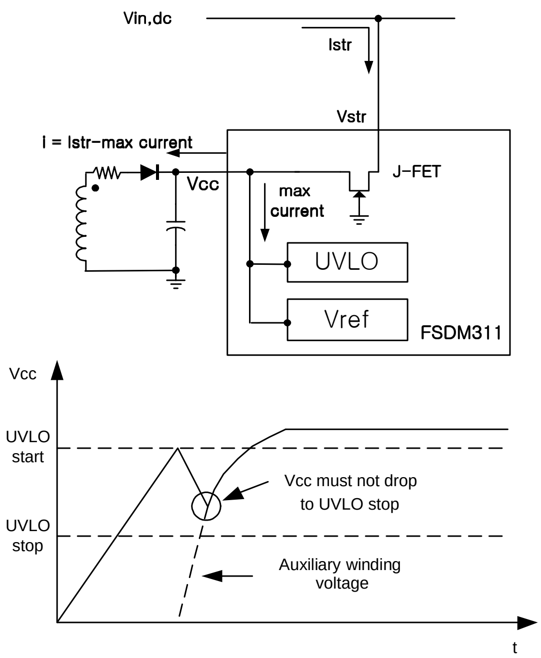


Figure 5. Charging the Vcc capacitor through Vstr

2. Feedback Control : The FSDM311 are the voltage mode devices as shown in Figure 6. Usually, an opto-coupler and KA431 type voltage reference are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform. This directly controls the duty cycle. When the KA431 reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increase pulling down the feedback voltage and reducing the duty cycle. This will happen when the input voltage increases or the output load decreases.

3. Leading edge blanking (LEB) : When the MOSFET is turned on, there usually exists a high current spike through the MOSFET. This is caused by primary side capacitance and secondary side rectifier reverse recovery. This could cause premature termination of the switching pulse if it exceeded the over-current threshold. Therefore, the FPS employs the leading edge blanking (LEB) circuit. This circuit inhibits the over current comparator for a short time after the MOSFET is turned on.

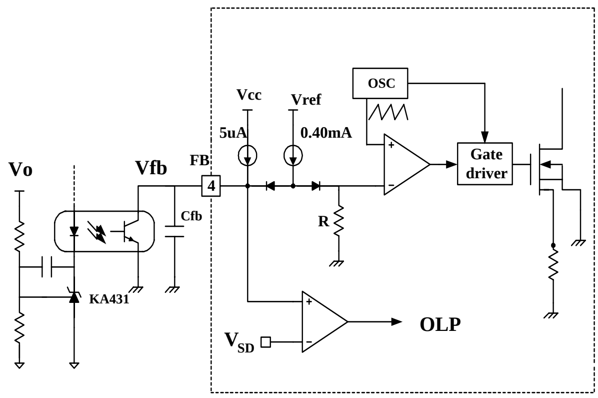


Figure 6. PWM and feedback circuit

4. Protection Circuit : The FSDM311 has 3self protection functions: over-load protection (OLP), thermal shutdown (TSD) and over-voltage protection. Because these protection circuits are fully integrated into the IC with no external components, system reliability is improved without cost increase. If either of these functions are triggered, the FPS starts an auto-restart cycle. Once the fault condition occurs, switching is terminated and the MOSFET remains off. This cause Vcc to fall. When Vcc reaches the UVLO stop voltage (7V), the protection is reset and the internal high voltage current source charges the Vcc capacitor. When Vcc reaches the UVLO start voltage (9V), the device attempts to resume normal operation. If the fault condition is no longer present start up will be successful. If it is still present the cycle is repeated. This is shown in Figure 7.

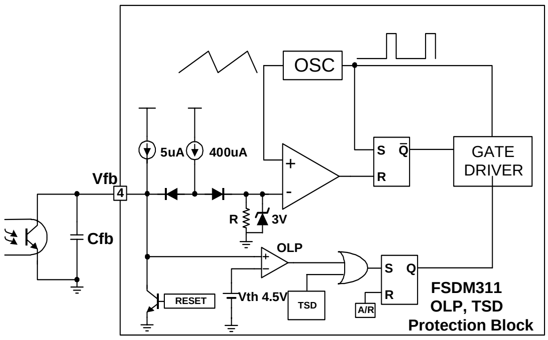


Figure 7. Protection block

4.1 Over Load Protection (OLP) : Overload is a load current that exceeds a pre-set level due to an abnormal situation. If this occurs, the protection circuit should be triggered to protect the SMPS. It is possible that a short term load transient can occur under normal operation. If this occurs the system should not shut down. In order to avoid false shutdowns, the over load protection circuit is designed to trigger after a delay. Therefore the device can discriminate between transient overloads and true fault conditions. The device is pulse-by-pulse current limited and therefore, for a given input voltage, the maximum input power is limited. If the load tries to draw more than this, the output voltage will drop below its set value. This reduces the opto-coupler LED current which in turn will reduce the photo-transistor current. Therefore, the 400uA current source will charge the feedback pin capacitor, Cfb, and the feedback voltage, Vfb, will increase. The input to the feedback comparator is clamped at around 3V. Therefore, once Vfb reaches 3V, the device is switching at maximum power. At this point the 400uA current source is blocked and the 5uA source continues to charge Cfb. Once Vfb reaches 4.5V, switching stops. Therefore the shutdown delay time is set by the time required to charge Cfb from 3V to 4.5V with 5uA as shown in Fig. 5.

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are assembled in one package. This makes it easy for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 145°C, thermal shutdown is activated.

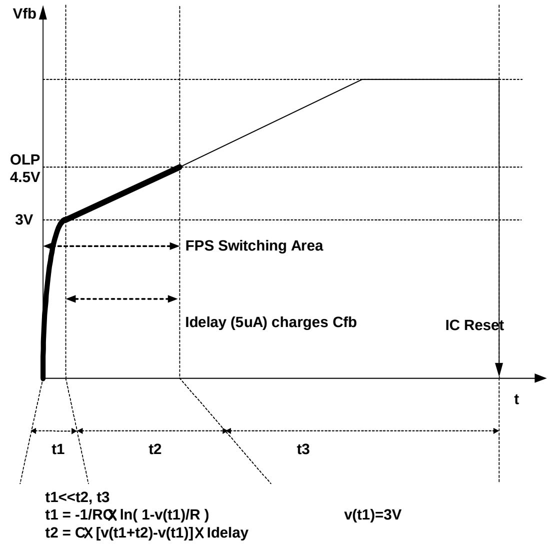


Figure 8. Over load protection delay

5. Soft Start : The FPS has an internal soft start circuit that increases the drain current limit together with the MOSFET current slowly after it starts up. The soft start time is typical 15msec as shown in figure 9. It progressively increases during the start-up phase. The pulse width to the power switching devices is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. Consequently it prevents the transformer's saturation and the secondary diodes's stress.

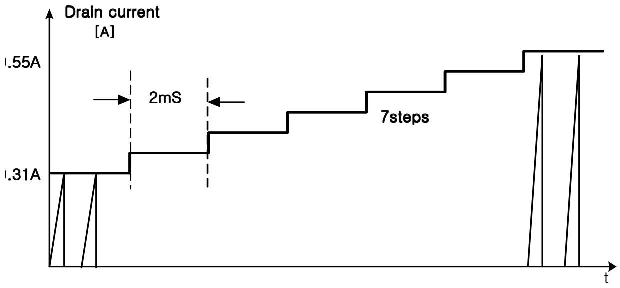


Figure 9. Internal Soft Start

6. Burst operation : In order to minimize the power dissipation in standby mode, the FSDM311 implements burst mode.

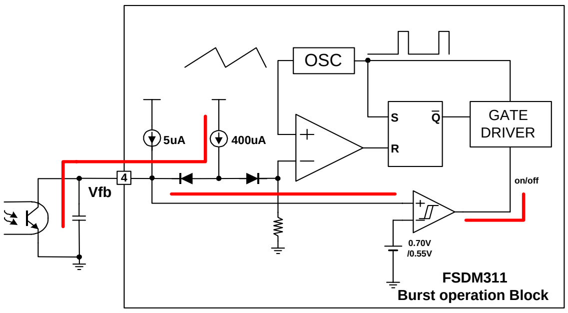


Figure 10. Circuit for burst operation

As the load decreases, the feedback voltage decreases. The device automatically enters burst mode when the feedback voltage drops below V_{BURL}(0.55V). At this point switching stops and the output voltages start to drop. This causes the feedback voltage to rise. Once is passes V_{BURH}(0.70V) switching starts again. The feedback voltage falls and the process repeats. Burst mode operation alternately enables and disables switching of the power MOSFET to reduce the switching loss in the standby mode.

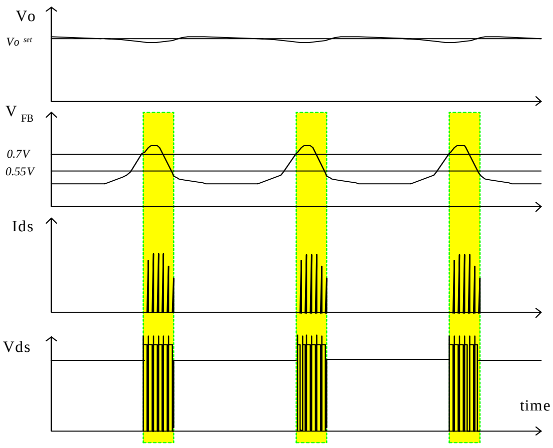
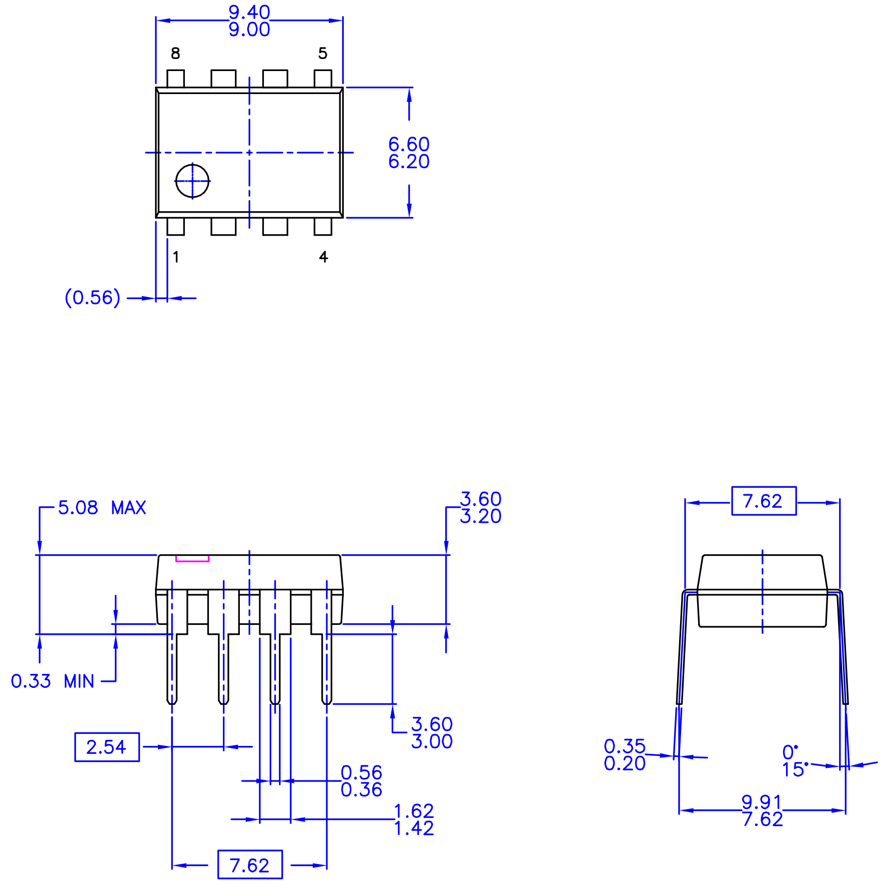


Figure 11. Burst mode operation

Package Dimensions

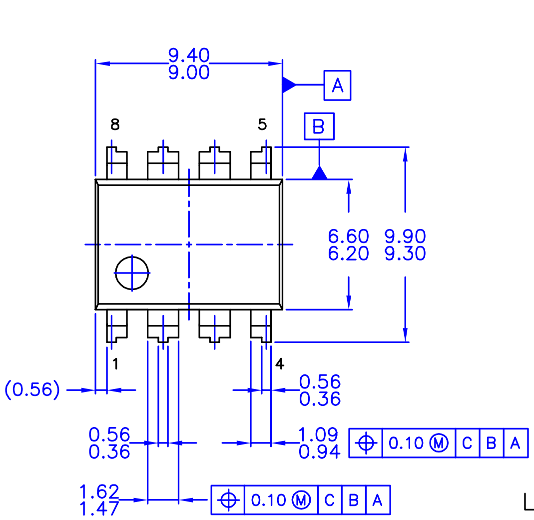
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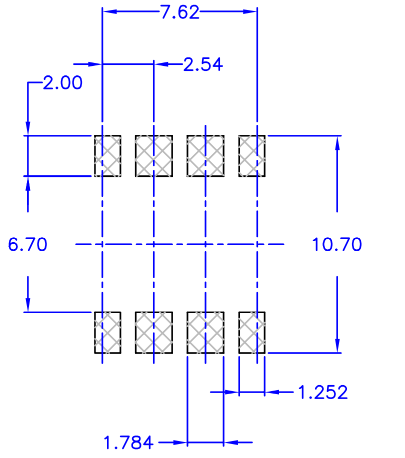


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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5M–1994

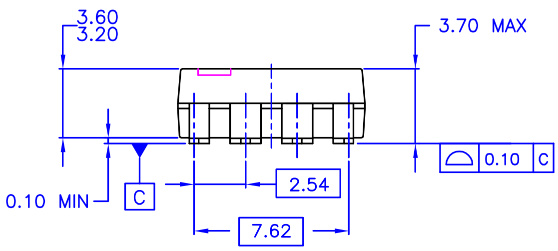
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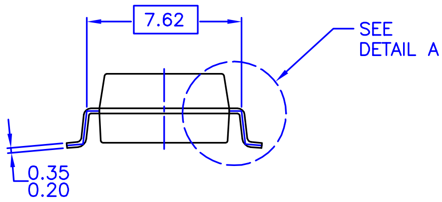
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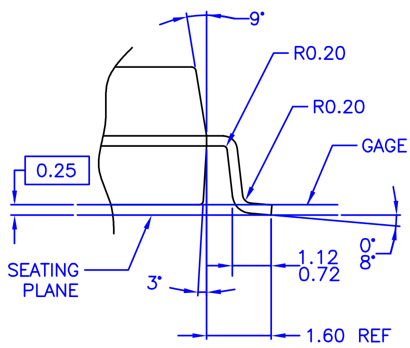




LAND PATTERN RECOMMENDATION







DETAIL A
SCALE: 2X

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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994

Ordering Information

Product Number	Package	Marking Code	Topr (°C)
FSDM311	8DIP	DM311	650V
FSDM311L	8LSOP	DM311	650V

DISCLAIMER

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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